جامعة الخليج للعلوم والتكنولوجيا GUST SINCE 2002 Gulf University For Science & Technology

Department of Computer Science

CSC 230 Digital Systems

(3 contact hours – 2 lab hours – 4 credits)

Syllabus[1]

- **General Information**

Instructor	
Office	
Phone	
Class Time	
Class Location	
Office Hours	
Teaching Assistant	

- **Required Textbook**

  Digital Design with RTL Design, VHDL, and Verilog, *Second Edition,* Frank Vahid, Wiley, 2011, ISBN: 978-0470531082.

- **Supplementary Textbook**

  Digital Systems: Principles and Applications, *Eleventh Edition*, R. Tocci, N. Widmer and G. Moss, Prentice Hall, 2011, ISBN: 9780135103821.

- **Course Description**

  Introductory course in digital logic and its specification and simulation. Number systems. Binary arithmetic. Boolean algebra. Combinational logic design. Sequential logic design (controllers). Data path components (e.g. Registers, adders, register files, etc.). Memory components (e.g. RAM, ROM). Register-transfer level (RTL) design.

- **Course Prerequisites**

  CSC125 (Introduction to Computing)

- **Course Category**

  Required

[1] **This syllabus may change as needed. In such a case, students will be informed accordingly**

- **Course Outcomes:**

At the completion of this course, students will be able to:

1. Convert numbers from one base to another, and add/subtract numbers represented in binary and twos complement form. [ABET a].
2. Apply the principles of Boolean algebra to design digital circuits. [ABET a].
3. Analyze and design combinational and sequential logic circuits. [ABET c].
4. Design special-purpose processors using RTL design. [ABET a, c].
5. Describe and use memory components (e.g. RAM, ROM, etc.). [ABET a].
6. Use computer-aided design (CAD) tools for digital logic design with FPGAs as the implementation technology. (Lab) [ABET i].
7. Work effectively in teams. (Lab) [ABET d].
8. Communicate effectively. (Lab) [ABET f].

- **Tentative Schedule**

Topic	**Week**
Syllabus	1
Ch1: Introduction and Number Systems.	1-2
Ch2: Boolean Algebra and Combinational logic design.	3-5
Ch3: Sequential logic design -- Controllers	6,7
Ch4: Datapath components and Binary Arithmetic	8-10
Ch5: Register-transfer level (RTL) design	11-14
Ch6: Optimizations and tradeoffs (if time permits)	15

- **Grading Scheme**

Quizzes	**10%**
Assignments	**5%**
Laboratory work	**25%**
Midterm Exam	**25%**
Final Exam	**35%**